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<tr>
<td>E000-EFFF</td>
<td>R</td>
<td>D D D D D D D D D</td>
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<td>I/O 1</td>
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<td>6600</td>
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<tr>
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<td>R R W D D D D D D D D</td>
<td>V RAM</td>
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Descriptions of Black Widow Printed Circuit Board Names

A10, A13-A15
Address bits on Microprocessor Address Bus lines A10 and A13-A15 are generated by Microprocessor C2. Bits on lines A13-A15, together with A16, are the input bits to Address Decoders R1-R2. A10 is exclusive-Orred with BANK SEL by gate 96 to produce the A10 input bit for Random-Access Memory N/P.

A80-A12
Address bits on Buffered Microprocessor Address Bus lines A80-A12 are software-generated by Microprocessor C2 and buffered by S1 and C1. These signals are Random-Access Memory Memories D1, E1, H1, J1, K1, and M1; and to Random-Access Memory N/P.

A86-A88 are the select input signals for Address Decoder P3.

Address bits A81-A12 and A13-A15 are the input bits for Address Decoders R1 and R2.

Address bits A80-A83 are applied with bits from AVG/AVG12 to Vector Address Selectors K8, K6, K8, and N8 to produce the data lines on Lines AM0-AM12.

Bits A80-A83 are control signals to custom audio chips B3 and C0/D3 in the Option Switch Input and Audio Output circuit.

Bits A80-A83 are the input signals to latch P2 in the High-Score table circuit where they are used to select the A14 address input for INEAR M2.

A13
A13 is from A81, inverted by J2, and applied to Vector Address Selector N6. When VMEM is low, A13 and A15 select the specific Video Memory Read-Only Memory.

AM0-AM13
Address bits on Multiplexed Address Bus Lines AM0-AM13 are software-generated by Vector Address Selectors K8, K6, K8, and N8. When VMEM is low, the Multiplexed Address Bus is from Buffered Microprocessor Address Bus A80 through A812 and A13. When VMEM is high, AM0-AM12 is from Vector-Address Generator Bus Lines AVG0-AVG12.

Signals AMO-AM11 are the input address signals to Vector Read-Only Memories L7, M7, N7, P7, R7, and to Vector-Random-Access Memory K7. In addition, AM11-AM13 are the select input signals for the Vector Address Decoder Circuit to decode the signal for multiplexers N3 and R5 of the State Machine circuit.

AUD 1-16
The Audio 1 and Audio 2 signals are game output producer signals that are generated by control signals and decoded by the Option Switch Input and Audio Output circuit, AUD 1 is the inverse of AUD 2. These signals are applied to the Audio/Regulator IC P8 and ultimately drive speakers 1 and 2.

AVG0-AVG12
Address bits on Vector-Generator Address Bus Lines AVG0-AVG12 are software-generated by Vector Address Decoder Control J8. When VMEM is high, these signals are passed through the Vector Address Selectors on lines AM0-AM13 to the Vector Read-Only Memory and to the Vector-Random-Access Memory.

BANK SEL
The Bank Select signal is developed from data on line DB2. When latch R9 of the Coin Door and Control Panel Output circuit is clocked by latch JR9, latch R9 of the Coin Door and Control Panel Output circuit latch the data bit on DB2 to pin 5 of R9. From here, the signal is current amplified and inverted by Q4 and applied to the utility Game Timer to activate the Left Coin Counter.

COIN CNTRL
Coin Counter Left is a game PCB output signal developed from the data on line DB6. When clocked by latch JR9, latch R9 of the Coin Door and Control Panel Output circuit latch the data bit on DB6 to pin 6 of R9. From here, the signal is current amplified and inverted by Q4 and applied to the utility Game Timer to activate the Right Coin Counter.

COIN LOCKOUT
Coin lockout is a game PCB output signal developed from the data on line DB3. When clocked by latch JR9, latch R9 of the Coin Door and Control Panel Output circuit latch the data bit on DB3 to pin 9 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Right and Left Lockout Coins of the game Coin Door.

DO/D7
Microprocessor Data Bus lines DO/D7 form a bi-directional data bus between the Microprocessor, the Read-Only Memory, and the Option Switch Input circuits.

DB0/DB7
Microprocessor Data Bus lines DB0-DB7 form a buffered bidirectional data bus between microprocessor data buffer P2 and Memory Memory Data Buffer P6. Coin Door and Control Panel Input buffer LS, M6, and N6. High-Score Table latches K2 and J2 and High-Score Table buffer H2.

DIS DAT
Disable Data is an active low-level signal generated by test equipment connected to the DiST DAT test point. DiST DAT is ANDed with the ROM signal by gate E3 to produce the enable signal for buffer E2 of the Read-Only Memory. When enabled, E2 passes data from the selected Read-Only Memory to the Microprocessor Data Bus.

DISRST
Display Reset is an active low-level signal software-generated by gate LS of the Halt Circuit. When either RESET or DISRST is low, DiST DAT is low. When low, DISRST clears State Memory latch P4, DAC Reference and Bipolar Current Sources latch E8, RGB Output latch K9, Vector Scaling latch O7, 2-Intensity, and Blanking latch E8 and counter M3. In addition, DISRST presets the HALT signal from latch LS to the high level.

DIGHO/DEV7
Data on Vector-Generator Data Bus lines DIGHO/DEV7 are software-generated by the selected Read-Only Memory or Random-Access Memory memory. If Memory Memory Data Buffer P6 is enabled (BUFFEN is low) and the RBW line is low, the data line on lines DIGHO/DEV7 is passed through P6 to the buffered Microprocessor Data Bus to be read by the microprocessor. Otherwise, the data on DIGHO/DEV7 is sent to the Vector Data Memories and to the Op Code and Instruction Latches.

DVX3-DVX12, DVX13
Data on Coin X Axis Vector Data Lines DVX3-DVX12 and DVX13 are software-generated by Vector Data Shifters 8B, 8C, and latch 6B of the Op Code and Instruction Latches. DVX3-DVX12 and DVX13 are the input signals to digital-to-analog converter G3. The data carry on these lines represents the X-axis change from the current location of the display beam. If DVX12 is low, DAC A/B operates only in its lower 12 positions, which means a negative direction of change on the display. If DVX13 is high, DAC A/B operates only in its upper 12 positions for a positive direction of change on the display.

In addition, DVX11 and DVX12 are exclusive-orred by gate 96 of the Normalization Flag circuit.

DYVDY/DVY2
Data bits on X-Axis Vector Data Lines DYVDY/DVY2 and DVY12 are software-generated by Vector Data Shifters 8F, 8H, 8J, and latch 6D of the Op Code and Identity Latches circuit. DYVDY-DVY11 and DVY12 are the input signals for digital-to-analog converter DAC F9 of the Y-Axis Output circuit. The data carried on these lines represents the Y-axis change from the current location of the display beam. If DYVDY is low, DAC F9 operates only in its lower 12 positions, which means a negative direction of change on the display. If DYVDY is high, DAC F9 operates only in its upper 12 positions for a positive direction of change on the display.

In addition, DVY10-11 are applied to latch E8 of the DAC Reference and Bipolar Current Sources circuit. These latches, together with VCIR and VCTR, set the X REF and Y REF voltage levels via DAC D6.

Lines DYVDY/DVY2 carry data representing the eight different color signals for latch K10 of the RGB Output circuit.

Lines DYVDY10/DVY12 carry data representing the Z-intensity signals for latch E8 of the Z-Intensity and Blanking circuit.

Data on DYVDY10/DYVDY12 are applied to latch D7 of the Vector Scaling circuit. The data carried on these lines represents the number (in binary) that the Vector Scaling circuit uses to divide into the vector drawing time. The vector drawing time is divided by 2, w here n equals the number represented on DYVDY10/DYVDY11.

In addition, DYVDY11 and DYVDY12 are exclusive-orred by gate 96 of the Normalization Flag circuit.

EARMOM
The Electrically-Attable ROM Control signal is an active low-level signal generated by Address Decoder P3 at address 8600. EARMOM is the clock signal for latch K1 in the High-Score Table circuit. EARMOM allows K2 to pass data on lines DB6/7 to the control lines of EARMOM M2.

EARMORD
The Electrically-Attable ROM Read Enable is an active low-level signal software-generated by Address Decoder R2 at address 7XXX. EARMORD is the clock signal for latches J2 and P2 in the High-Score Table circuit. EARMORD allows address bits on DB0 and adds bits on data lines DB6/7 to pass to the address and data input pins of EARMOM M2.

EARMWR
The Electrically-Attable ROM Write Enable is an active low-level signal software-generated by Address Decoder P3 at address 8940. EARMWR is the clock signal for latches J2 and P2 in the High-Score Table circuit. EARMWR allows address bits on DB0-ABS and data bits on lines DB6/7 to pass to the address and data input pins of EARMOM M2.
The active high-level Normalization Flag is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data line on D5V4-DVY7 is high, OP1 is set when high is clocked by LATCH1. OP1 is multiplexed with a high N4 in the State Machine circuit to produce the A5 input address bit for State Machine ROM N4. In addition, OP1 is the OP input signal for Vector Address Controller J9.

In the Vector Timer circuit, OP1 is gated by K5 and E3 to enable a 110 to be loaded into the D input pin of Vector Timer P6 (if NORM is true).

The Complementary Op Code 1 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP1. If OP1 is high, then NORM is generated by loading the data lines on D5V4-DVY7 at the clock of E5 when high is clocked by LATCH1. This signal is also the input signal for latch D6.

**Normal**

The active low-level signal is software-generated by decoder H7 of the State Machine circuit. LATCH3 is applied through invertor F7 to the 50 input pins of shift register B8 in the Vector Data Shifters circuit. LATCH3 causes the data bits on lines D5V5-DVY3 to be latched by B8 and O6 to lines D5V3-DVY7 when B6 is clocked by the 12MHz clock signal.

Invert Y

Invert Y is an active high-level signal generated from the data bit on line D5V6. When clocked by LATCH1, latch R9 of the Coin Door and Control Panel Output circuit latches DB7 to pin 15 of R9. LABD8 closes switch S10 through invertor K9 in the Y-Axis Output circuit. This inverts the Y-axis vector instruction to the display.

**Input/Output**

The Input/Output signal is an active low-level signal software-generated by Address Decoder R2 during addresses 6000 through 6E7F. **INPUT** is NORM is applied with right 16 by 8 Westgate System ROM N4.

**Green**

Green is a game output pin signal generated from the data line on D5V1 in the O-B-A Output circuit. When D5V1 is high and latch K10 is clocked by STATU, D5V1 on D5V1 is inverted and latched to pin 6 of K10. If both BLANK1 and BLANK2 are low, this data bit is again inverted by gate L10 to line Q8. Transistor Q8 generates the GREEN signal for the display.

**Hal**

The active high-level Halte Flag is software-generated by latch L5 of the Halt Flag circuit. Halt is applied through buffer control of the Coin Door and Control Panel Input Circuit (when SINPI is high) to permit Microprocessor C3 in the State Machine circuit to power down latch D6. In addition, HALT is latched to latch P4 of the State Machine circuit to develop HALT.

**Halt**

The active high-level Delayed Halt Flag is software-generated by latch P4 of the State Machine circuit. **HALT** is generated when the HALT signal has been delayed by one pulse of inverted VCC (15.6MHz), which in turn has been delayed by one pulse of 12 MHz. **HALT** is reset with gate O by gate Y of the State Machine circuit to prevent the A7 input address bit for ROM M4.

**Halt**

The active low-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. Halt is applied through buffer control of the Coin Door and Control Panel Input Circuit (when SINPI is high) to permit Microprocessor C3 in the State Machine circuit to power down latch D6. In addition, HALT is reset with CNTRY by gate L5 of the Center Flag circuit to produce CENTRY.

**Interc**

Interrupt Acknowledge is an active low-level signal software-generated from Microprocessor C2 that an interrupt request has been received. **INTER** resets counter J4.

**Invert**

Invert X is an active high-level signal developed from the data bit on line D5V6. When clocked by LATCH1, latch R9 of the Coin Door and Control Panel Output circuit latches DB7 to pin 15 of R9. LABD8 closes switch S10 through invertor K9 in the X-Axis Output circuit. This inverts the X-axis vector instruction to the display.

**Latch**

Latch 3 is an active low-level signal generated by decoder H7 of the State Machine circuit. LATCH3 is applied through invertor F7 to the 50 input pins of shift register B8 in the Vector Data Shifters circuit. LATCH3 causes the data bits on lines D5V4-DVY3 to be latched by B8 to lines D5V3-DVY7 when B6 is clocked by the 12MHz clock signal.

**LLatch**

LATCH2 is also the clock signal for Op Code and Intensity Latch O6. When LATCH2 is low, the data bits on lines D5V4-DVY3 are latched by O6 to lines O5V3-O5V7, D5V2, and D5V5.

**Normal**

The high active-level Normalization Flag is software-generated by latch A6 in the Normalization Flag circuit. If OP1 is high, NORM is set high when STROBED goes high. NORM is generated with byte K5 in the Vector Timer circuit to produce the load-enable signal. If latch D6 is 1, latch D3 is enabled, NORM initiates the divide-by-2 operation of the vector drawing time. (The n factor is specified by the data lines on D5V4-DVY10 to Vector Scaling latch D7.)

**Option 2**

The Option 0, Option 1, and Option 2 signals are hardware-generated. The OP switch P10. They are applied to switch input buffer L9 of the Coin Door and Control Panel circuit. When L5 is enabled, INVERT Y is applied to Buffer. Microprocessor Data Bus lines D5V4-D5V7.

**Op**

The Op Code 0 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data line on D5V5 is high, OP1 is set when high is clocked by LATCH1. OP1 is the A4X input signal to the State Machine circuit to produce the A4 input address bit for ROM M4.

**Op1**

If OP1 is high, HALT from Halt Flag latch L5 is set when high is clocked by LATCH1. If OP1 is high, latch L5 is clocked by STROBED.

**Op2**

If OP1, OP2, STROBED, and VGCK are all low, VCIF from Vector latch flag E5 is set when high is clocked by the 12MHz clock signal.

**Strobe**

When STROBED goes low, E5 is low. It is applied through gates B7 and F3 of the Vector Scaling circuit as the load signal for counter C7. This signal is latched from D5V4-DVY7 by D7 to be loaded into counter C7. When STROBED goes high, counter C7 reaches its maximum count. At the same time, the Vector Timer circuit does a divide-by-2 right shift operation for each count of C7. (This is caused by SCALE being at the high level and C7 being high for the maximum count. When C7 reaches its maximum count, it sets pin 12 high, dropping SCALE to the low state.

If OP2 and STROBE is low, VCIF from gate A6 is set when low is set when STROBED goes low. This allows Vector Scaling latch D7 to latch the new data on D5V4-DVY7.

**Op2**

When E5 and D5V4-DVY7 are low, SCALE is set low. SCALE is set low when STROBED goes low. This allows latch E6 of the Z Intensity and Blanking circuit to latch the data on D5V4-DVY7.
Black Widow PCB Signal Name Descriptions, cont.

PLAYER 1 LED
The Player 1 LED ON signal is developed from the data bit on line DB4. When clocked by CATCH1, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on line DB4 to pin 19 or R9. This signal is applied through R10 to light the Player 1 LED on the game Control Panel.

PLAYER 2 LED
The Player 2 LED ON signal is developed from the data bit on line DB5. When clocked by CATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB5 to pin 16 or R9. This signal is applied through R12 to light the Player 2 LED on the game Control Panel.

POD
The active high level Power-On Reset signal is hardware-generated at pin 4 of F7 in the Power-On Reset circuit. POD is a reset signal that starts the count of 4 of the Clock circuit.

POD
The active low level Power-On Reset signal is hardware-generated at pin 6 of inverter F7 in the Power-On Reset circuit. POD is generated when the voltage at pin 3 of R6 is less than about 7 volts or when the reset test point is shorted to ground. POD is developed into the RESISTOR signal to protect Microprocessor C2.

RAH
The Random-Access Memory Enable is an active low level signal generated by Address Decoder D2 during addresses 0000 through 01FF. RAH is the chipenable signal for Random-Access Memory N1. When low, RAH allows data to be read from or written to N1P1, depending upon the state of WRTE.

RED
Red is a game PCB output signal developed from the data bit on line D3 in the 4G + Output Circuit. When D3 is high and latch K12 is not clocked by T1 in the Watchdog circuit, RED is low and latched to pin 3 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate G10 to run on Q6. Transistor Q6 generates the RED signal for the display.

RESET
Reset is an active low level signal generated at pin 6 of K3 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets RESET to an active low level either when the reset test point is shorted to ground or during the time that the power-supply voltages are required to be regulated levels. This ensures that the Microprocessor Address Bus is stabilized before the microprocessor begins operation.

The Watchdog circuit sets RESET to an active low level if the microprocessor fails to output address 0000 before the Watchdog counter N4 has reached its maximum count. RESET is also the clear signal for latch R9 in the Coin Door and Control Panel Output circuit. In addition, RESET is gated with VNEG by gate L6 in the Halt Flag circuit to produce DISRT.

ROM
The Read-Only Memory Enable is an active high level signal generated from Address Decoder D1 during addresses 0000 through 3FFF. ROM is edged by IOS with gate G4 to enable bidirectional data bus buffer G2 to pass data.

In addition, ROM is ANDed with DISRT to enable data buffer E2.

ROM
Read-Only Memory Chip Select 0 is an active low level signal generated by Address Decoder R1 at addresses 9000 through DF7 in the Read-Only Memory circuit. When low, ROMD allows ROM D1 to be addressed and to pass data to buffer E2.

ROM
Read-Only Memory Chip Select 1 is an active low level signal generated by Address Decoder R1 at addresses A000 through E7F in the Read-Only Memory circuit. When low, ROME allows ROM E1 to be addressed and to pass data to buffer E2.

ROM
Read-Only Memory Chip Select 2 is an active low level signal generated by Address Decoder R1 at addresses 8000 through B7F in the Read-Only Memory circuit. When low, ROMF allows ROM F1 to be addressed and to pass data to buffer E2.

ROM
Read-Only Memory Chip Select 3 is an active low level signal generated by Address Decoder R1 at addresses C000 through FF7 in the Read-Only Memory circuit. When low, ROMG allows ROM G1 to be addressed and to pass data to buffer E2.

ROM
Read-Only Memory Chip Select 4 is an active low level signal generated by Address Decoder R1 at addresses 0000 through 01FF in the Read-Only Memory circuit. When low, ROMH allows ROM H1 to be addressed and to pass data to buffer E2.

ROM
Read-Only Memory Chip Select 5 is an active low level signal generated by Address Decoder R1 at addresses 0000 through E7F in the Read-Only Memory circuit. When low, ROMJ allows ROM J1 to be addressed and to pass data to buffer E2.

ROM
Read-Only Memory Chip Select 5 is an active low level signal generated by Address Decoder R1 at addresses 0000 through E7F in the Read-Only Memory circuit. When low, ROMK allows ROM K1 to be addressed and to pass data to buffer E2.

ROM
Read-Only Memory Chip Select 5 is an active low level signal generated by Address Decoder R1 at addresses 0000 through E7F in the Read-Only Memory circuit. When low, ROML allows ROM L1 to be addressed and to pass data to buffer E2.

ROM
Although ReadWrite Enable is enabled by Microprocessor C2, buffered by B1, and applied as the read/write enable signal for custom audio circuits B3 and C3D of the Option Switch Input and Audio Output circuit, in the high state, R/W is the read enable for the custom audio circuits; in the low state, it is the write enable for these circuits.

ROM
The Buffered ReadWrite Enable is enabled by Microprocessor C2, buffered by B1, and applied as the read/write enable signal for custom audio circuits B3 and C3D of the Option Switch Input and Audio Output circuit. In the high state, R/W is the read enable for the custom audio circuits; in the low state, it is the write enable for these circuits.

SA
The active high level Signature Analytic Flag signal is hardware-generated at test point SA at pin 11 of J3 is grounded. SA is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

SA
Signature Analytic Clock is a test point at pin 8 of gate G7 in the State Machine Clock Logic circuit. SACLK is used to apply the clock signal from the Signature Analyzer or ATARI CAT Box for the reading of game PCB signatures.

SA
Signature Enable is a test point at pin 8 of gate G7 in the Vector Address Selector circuit. SAEN is generated by gating VRAM with the data bit on line A14M by gates J3 and M5. SAEN is used to enable a Signature Analyzer or the CAT Box for the reading of game PCB signatures.

SA
Signature Enable is a test point at pin 8 of gate G7 in the Vector Address Selector circuit. SAEN is generated by gating VRAM with the data bit on line A14M by gates J3 and M5. SAEN is used to enable a Signature Analyzer or the ATARI CAT Box for the reading of game PCB signatures.

SA
The active low level Signature Analytic Flag is hardware-generated at test point SA at pin 11 of J3 is grounded. SA is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

SACLK
Signature Analytic Clock is a test point at pin 8 of gate G7 in the State Machine Clock Logic circuit. SACLK is used to apply the clock signal from the Signature Analyzer or ATARI CAT Box for the reading of game PCB signatures.

SCALE
Scale is an active high level signal generated by gate B7 of the Vector Scaling circuit. When G2 is high and connect G7 is not counting down, SCALE is set high. SCALE is ORed with NORM by gate K5 of the Vector Timer circuit to produce the load signal for Vector Timers M6, M6, and K6. When SCALE is high, the Vector Timers perform a load operation for each count of G7 at a 124Hz rate. This results in a vector drawing time divided by a factor of 2, where n equals the total counts of G7. When G7 reaches its minimum count, SCALE is set low.

SCALE
SCALE is gated with VCTR, CNTR, DTV11-DVY12, and DTV11-DVY12 of the Normalization Flag circuit to produce the clear signal for latch J6.

SCALE
Scale Load is an active low level signal generated by gates N5, L5, and L6 of the Vector Generator. When VCTR, CNTR, G2, and DTV11-DVY12 are both high, SCALE is set.

SCALE
SCALE is the clock signal for Vector Scaling latch 07. When SCALE goes high, the data on lines DTV10-DVY12 are latched to the output pins of D7.

SNFP
Switch Input 1 is an active low level signal generated by Address Decoder R2 at address 6000. SNF1 is the direction signal for bi-directional data buffer N6 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer N6.

SNFP
Switch Input 2 is an active low level signal generated by Address Decoder R2 at address 6000. SNF2 is the direction signal for bi-directional data buffer N6 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer N6.
Black Widow PCB Signal Name Descriptions, cont.

ST3
State signal ST3 is an active high-level signal generated by Decoder Decoder latch A1. ST3 is opposite in state to VGOQ, and is delayed by one pulse of the 12.6 MHz clock signal if the G4 output from State Machine ROM H4 is low and VMEM is high. If the G4 output from H4 is high, ST3 is high. When ST3 is high, State Machine decoder H7 is disabled. When ST3 is low, H7 enables the input on lines ST0-ST7 to produce LATCH1/LATCH2 and STROBEO/STROBE2.

VCIR, VCIR
The Vector Flag signals are software-generated by Vector Flag latch E5, I/Os, DQS, STROBEO, and VGOQ and are low and FA7 is high. VCIR is set high and VCIR is set low when E5 is clocked by the 12.6 MHz clock signal. VCIR is Oifred with CNTR by gate M6 to set GO high.

SCALE, CNTR, DSV1/DV12, and DSV1/DV12 are gated with VCIR to produce the clear signal for Normalization Flag latch A6. In the Z Intensity and Blanking circuit, the VCIR clock is for latch H6 and the serial input signal for write register M3.

VCIR and VCR are used by the DAC Reference and Bipolar Current Sources circuit to set X BIP, Y BIP, X REF, and Y REF data.

VGOQ
The Vector Generator clock signal is generated at pin 18 of bus 1 in the Microprocessor circuit. VGOQ is derived from the 12.6 MHz clock signal and is applied to AND gate J5 of the State Machine Clock Logic circuit. VGOQ is the basic timing signal of the State Machine circuit.

VGOO
The Vector Generator Go signal is an active low-level signal software-generated by Address Decoder P3 at address 8860. VGOO is the clear signal for latch 56 of the Heat Flag circuit. When low, VGOO sets HALT to the inactive low level.

VGOO
Vector Generator Reset is an active low-level signal software-generated by Address Decoder P3 at address 8860. VGOO is driven with RESET by gate 56 of the Heat Flag circuit to produce DISRG.

VMEM
The Vector Memory Select Enable is an active low-level signal software-generated by Address Decoder P3 at address 8860. VMEM is the select-enable signal for Vector Address Selectors K6, L6, M6, and N6. When low, VMEM allows the Vector Address Selectors to produce WR, BUFFER, and the AM/AM12 multiplexed address bits. VMEM is also applied to gate K5 of the State Machine Clock Logic circuit where it is used to generate ST3.

VRAM
The Vector Random-Access Memory Chip Enable is an active low-level signal software-generated by Address Decoder P3 at address 8860. VRAM is driven with RESET by gate 56 of the Heat Flag circuit to produce DISRG.

VROM0
Vector Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2600-2FFF. VROM0 is the chip-select signal for ROM L7 of the Vector Read-Only Memory circuit. When low, VROM0 allows ROM L7 to be addressed and to pass data to the Vector Generator Data Bus.

VROM1
Vector Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 3000-3FFF. VROM1 is the chip-select signal for ROM M/7 of the Vector Read-Only Memory circuit. When low, VROM1 allows ROM M/7 to be addressed and to pass data to the Vector Generator Data Bus.

VROM2
Vector Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 4000-4FFF. VROM0 is the chip-select signal for ROM N/7 of the Vector Read-Only Memory circuit. When low, VROM allows ROM N/7 to be addressed and to pass data to the Vector Generator Data Bus.

VROM3
Vector Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 5000-5FFF. VROM3 is the chip-select signal for ROM O/7 of the Vector Read-Only Memory circuit. When low, VROM3 allows ROM O/7 to be addressed and to pass data to the Vector Generator Data Bus.

VW
The Vector Write Enable is an active low-level signal software-generated by Vector Address Selector K8, ANDed with HB8 by gate J6, and applied as the writeenable signal for Vector Random-Access Memory K7. When low, VW allows data to be written to K7; when high, VW permits data to be read from K7.

WDCLR
Watchdog Clear is an active low-level signal software-generated by Address Decoder P3 at address 8980. WDCLR is Oifred with POR by gate E3 to clear the count of Watchdog counter H4.

WDODE
Watchdog Disable is a test point at pin 9 of AND gate L4 in the watchdog circuit. When WDODE is grounded, RESET is prevented from going to an active low level (except when the RESET test point is grounded).

WRITE
Write Enable is an active low-level signal generated by gate K4 of the Microprocessor circuit. WRITE is used to enable Address Decoder P3 and Random-Access Memory N/7. WRITE is also applied to pin 11 of K8 in the Vector Address Selector circuit to develop X BIP.

X BIP
The X-Axis Bipolar Current is set by R98 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 16 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

X OUT
X Output is a game PCB output signal generated by the X-Axis Output circuit. X OUT carries the horizontal beam deflection signal for the drawing of vectors on the display.

X REF
The X-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

Y BIP
The Y-Axis Bipolar Current is set by R98 of the DAC Reference and Bipolar Current Sources circuit. This is the reference current source for pin 16 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Y OUT
Y Output is a game PCB output signal generated by the Y-Axis Output circuit. Y OUT carries the vertical beam deflection signal for the drawing of vectors on the display.

Y REF
The Y-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

20-Z2, 21-Z2
Intensities Z0-2Z and Z1-2Z are software-generated by latch 0B in the Gro Code and Intensity Latches circuit. These signals are derived from the data on lines D0-0/D0V7 when CE is clocked bylATCH3. If the binary count carried by Z0-2Z is not equal to 1, these signals are the input signals for latch 0Z in the Z Intensity and Blanking circuit. If the binary count carried by Z0-2Z is 1, 2 intensity signals 20, 21, and 22 are ANDed by gate K5 of the

2 Intensity and Blanking circuit to produce the select signal for latch 0F. This select signal causes the latched data from 0E to be applied as the input signals for latch 0F.

2 Z OUT
2 Z Intensity Output is a game PCB output signal generated by the Z Intensity and Blanking circuit from either DTV/DTV2 or D2-Z. The 0 outputs from latch 0H are summed at the base of G7. Transistors G7 and 0 buffer 2 OUT before it is sent to the game display circuit to control the display Intensity.

3 KHZ
The 3 kHz clock signal is generated at pin 6 of Clock counter F4 and is applied through switch input buffer 09 of the Control and Control Panel Input circuit (when S10P is low). The 3 kHz clock output is derived from the data line of the 80. This frequency is the time reference for the Microprocessor C2.

12 KHZ
The 12 kHz clock signal is generated at pin 4 of Clock counter F4 and is applied to reset A4 of the High-Score Table.

3 MHz
The 3 MHz clock signal is generated at pin 2 of Clock counter F4. The 3 MHz signal is ANDed with RB8 and HB8 by gate K4 to produce WRITE. It is also applied to AND gate J5 of the State Machine Clock Logic and to shift register M3 of the Z Intensity and Blanking circuit.

6 MHz
The 6 MHz clock signal is generated at pin 3 of Clock counter F4 and is applied to gate J5 of the State Machine Clock Logic circuit.

12 MHz
The 12 MHz clock signal is generated at pin 10 of Inverter F3 in the Clock circuit. This signal clocks the Timer Shifters, the Vector Flag latch, and the Center Flag latch.
Adjusting X- and Y-Axis Video Potentiometers

If you replace the main Gravitar PCB or the display, you may have to make the following adjustments:

1. Enter self-test and advance to diagonal crosshatch pattern (Screen 2).
2. Centering Pots: Adjust X CENTER (R189) and Y CENTER (R212) so that the crosshatch pattern is located at the middle of the screen.
3. Size Pots: Adjust XSIZE (R182) and YSIZE (R213) so that the crosshatch pattern exactly covers the whole visible screen.
4. Linearity Pots: Adjust XLIN (R187) and YLIN (R210) so that the diagonal lines are straight. Since the LIN pots change the size of the displayed picture on the screen, you may have to readjust the SIZE pots in order to get the correct adjustment.
5. Bipolar Pots: Advance to the self-test raster pattern (Screen 4). Adjust XBIP (R99) and YBIP (R88) for a 1-inch high horizontal raster in the center of the screen. Be sure the raster ends are square with the sides of the outer rectangle.
Amplifone Main Wiring Diagram

Amplifone High-Voltage PCB

Note: Unless otherwise specified:
1. All resistor values are in ohms.
2. All capacitor values are in µF.

WARNING
Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

Amplifone
Color X-Y Display Schematic
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GENERAL NOTES

1. Resistance values in ohms, ¼ watt, ±0.5%, unless otherwise noted. R = 1,000; M = 1,000,000
2. Capacitance value of 1 or less is in microfarads, unless otherwise noted.
3. *Q600 and Q606 are not in High-Voltage PCB.
4. All D.C. voltages are ±10% measured from point indicated to ground, using a high-impedance meter. Voltages are measured with no signal input and controls are in a normal operating position.
5. Circled numbers indicate location of waveform reading.
6. ZD100-101 uses 6N30600-007 zener diode in series with 340X2531-934 330-ohm resistor in early production models.
7. Use a 1,000:1 probe when measuring G2 (screen) or focus voltage.

WARNING
Components identified by shading have special characteristics important to safety and should be replaced only with identical types.

Wells Gardner
Color X-Y Display Schematic Diagram
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